

# 74ALVCH16240

## Low-Voltage 16-Bit Buffer with Bus Hold 1.8/2.5/3.3 V (3-State, Inverting)

The 74ALVCH16240 is an advanced performance, inverting 16-bit buffer. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems.

The 74ALVCH16240 is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16-bit operation. The 3-state outputs are controlled by an Output Enable ( $\overline{OEn}$ ) input for each nibble. When  $\overline{OEn}$  is LOW, the outputs are on. When  $\overline{OEn}$  is HIGH, the outputs are in the high impedance state. The data inputs include active bus-hold circuitry, eliminating the need for external pull-up resistors to hold unused or floating inputs at a valid logic state.

- Designed for Low Voltage Operation:  $V_{CC} = 1.65$  to  $3.6$  V
- 3.6 V Tolerant Inputs and Outputs
- High-Speed Operation: 3.0 ns Max for 3.0 to 3.6 V  
3.7 ns Max for 2.3 to 2.7 V  
6.0 ns Max for 1.65 to 1.95 V
- Static Drive:  $\pm 24$  mA Drive at 3.0 V  
 $\pm 12$  mA Drive at 2.3 V  
 $\pm 4$  mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- Includes Active Bus-Hold to Hold Unused or Floating Inputs at a Valid Logic State
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0$  V†
- Near Zero Static Supply Current in All Three Logic States (40  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds  $\pm 250$  mA @  $125^{\circ}$ C
- ESD Performance: Human Body Model >2000V; Machine Model >200V
- Second Source to Industry Standard 74ALVCH16240

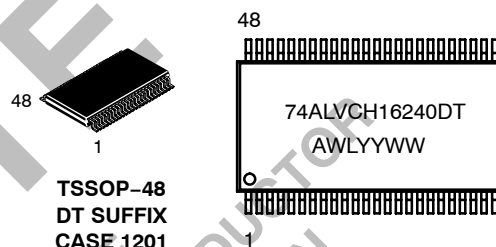
†To ensure the outputs activate in the 3-state condition, the output enable pins should be connected to  $V_{CC}$  through a pull-up resistor. The value of the resistor is determined by the current sinking capability of the output connected to the  $\overline{OE}$  pin.



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM

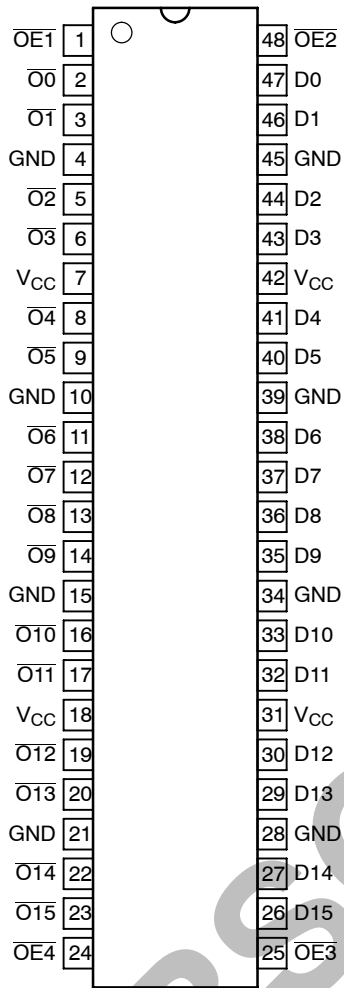


A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
74ALVCH16240DTR	TSSOP	2500 / Reel

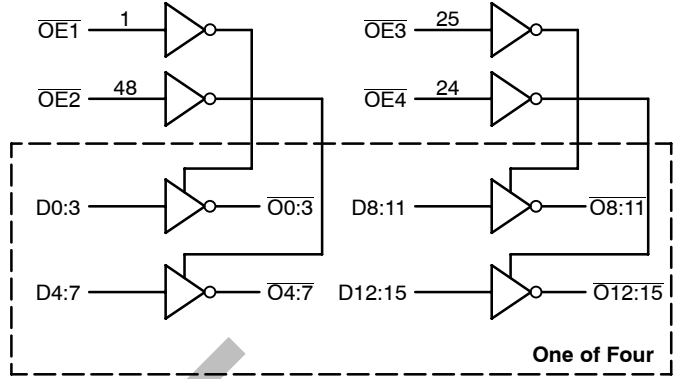
# 74ALVCH16240



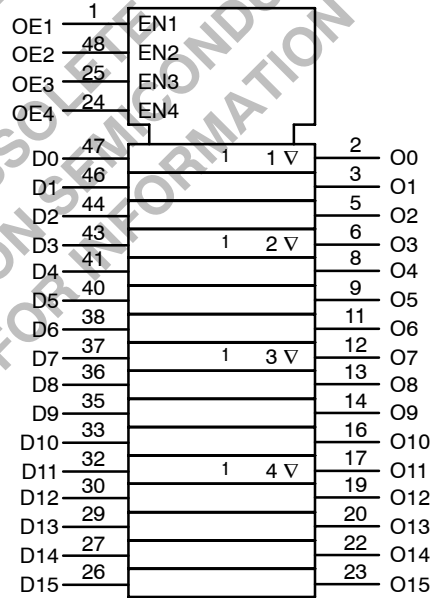
**Figure 1. 48-Lead Pinout (Top View)**

**PIN NAMES**

Pins	Function
$\overline{OE}_n$	Output Enable Inputs
D0–D15	Inputs
O0–O15	Outputs



**Figure 2. Logic Diagram**



**Figure 3. IEC Logic Diagram**

OE1	D0:3	O0:3	OE2	D4:7	O4:7	OE3	D8:11	O8:11	OE4	D12:15	O12:15
L	L	H	L	L	H	L	L	H	L	L	H
L	H	L	L	H	L	L	H	L	L	H	L
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level  
 L = Low Voltage Level  
 Z = High Impedance State  
 X = High or Low Voltage Level and Transitions Are Acceptable  
 For  $I_{CC}$  reasons, DO NOT FLOAT Inputs.

# 74ALVCH16240

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	- 0.5 to + 4.6	V
V <sub>I</sub>	DC Input Voltage	- 0.5 to + 4.6	V
V <sub>O</sub>	DC Output Voltage	- 0.5 to + 4.6	V
I <sub>IK</sub>	DC Input Diode Current V <sub>I</sub> < GND	- 50	mA
I <sub>OK</sub>	DC Output Diode Current V <sub>O</sub> < GND	- 50	mA
I <sub>O</sub>	DC Output Sink Current	± 50	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	± 100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	± 100	mA
T <sub>STG</sub>	Storage Temperature Range	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+ 150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2)	90	°C/W
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 30 to 35	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 N/A	V
I <sub>LATCH-UP</sub>	Latch-Up Performance Above V <sub>CC</sub> and Below GND at 125°C (Note 6)	± 250	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I<sub>O</sub> absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage Operating Data Retention Only	2.3 1.5	3.6 3.6	V
V <sub>I</sub>	Input Voltage (Note 7)	-0.5	3.6	V
V <sub>O</sub>	Output Voltage (Active State) (3-State)	0 0	3.6 3.6	V
T <sub>A</sub>	Operating Free-Air Temperature	- 40	+ 85	°C
Δt/ΔV	Input Transition Rise or Fall Rate V <sub>CC</sub> = 2.5 V ± 0.2 V V <sub>CC</sub> = 3.0 V ± 0.3 V	0 0	20 10	ns/V

7. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

# 74ALVCH16240

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
$V_{IH}$	HIGH Level Input Voltage (Note 8)	$1.65\text{ V} \leq V_{CC} < 2.3\text{ V}$	$0.65 \times V_{CC}$		V
		$2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	1.7		
		$2.7\text{ V} < V_{CC} \leq 3.6\text{ V}$	2.0		
$V_{IL}$	LOW Level Input Voltage (Note 8)	$1.65\text{ V} \leq V_{CC} < 2.3\text{ V}$		$0.35 \times V_{CC}$	V
		$2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$		0.7	
		$2.7\text{ V} < V_{CC} \leq 3.6\text{ V}$		0.8	
$V_{OH}$	HIGH Level Output Voltage	$1.65\text{ V} \leq V_{CC} \leq 3.6\text{ V}; I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 1.65\text{ V}; I_{OH} = -4\text{ mA}$	1.2		
		$V_{CC} = 2.3\text{ V}; I_{OH} = -6\text{ mA}$	2.0		
		$V_{CC} = 2.3\text{ V}; I_{OH} = -12\text{ mA}$	1.7		
		$V_{CC} = 2.7\text{ V}; I_{OH} = -12\text{ mA}$	2.2		
		$V_{CC} = 3.0\text{ V}; I_{OH} = -12\text{ mA}$	2.4		
		$V_{CC} = 3.0\text{ V}; I_{OH} = -24\text{ mA}$	2.0		
$V_{OL}$	LOW Level Output Voltage	$1.65\text{ V} \leq V_{CC} \leq 3.6\text{ V}; I_{OL} = 100\ \mu\text{A}$		0.2	V
		$V_{CC} = 1.65\text{ V}; I_{OL} = 4\text{ mA}$		0.45	
		$V_{CC} = 2.3\text{ V}; I_{OL} = 6\text{ mA}$		0.4	
		$V_{CC} = 2.3\text{ V}; I_{OL} = 12\text{ mA}$		0.7	
		$V_{CC} = 2.7\text{ V}; I_{OL} = 12\text{ mA}$		0.4	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 24\text{ mA}$		0.55	
$I_I$	Input Leakage Current	$1.65\text{ V} \leq V_{CC} \leq 3.6\text{ V}; 0\text{ V} \leq V_I \leq 3.6\text{ V}$		$\pm 5.0$	$\mu\text{A}$
$I_{I(\text{HOLD})}$	Minimum Bus-hold Input Current	$V_{CC} = 3.6\text{ V}; V_{IN} = 0\text{ to } 3.6\text{ V}$		$\pm 500$	$\mu\text{A}$
		$V_{CC} = 3.0\text{ V}; V_{IN} = 0.8\text{ V}$	75		
		$V_{CC} = 3.0\text{ V}; V_{IN} = 2.0\text{ V}$	-75		
		$V_{CC} = 2.3\text{ V}; V_{IN} = 0.7\text{ V}$	45		
		$V_{CC} = 2.3\text{ V}; V_{IN} = 1.7\text{ V}$	-45		
		$V_{CC} = 1.65\text{ V}; V_{IN} = 0.58\text{ V}$	25		
		$V_{CC} = 1.65\text{ V}; V_{IN} = 1.07\text{ V}$	-25		
$I_{OZ}$	3-State Output Current	$1.65\text{ V} \leq V_{CC} \leq 3.6\text{ V}; 0\text{ V} \leq V_O \leq 3.6\text{ V}; V_I = V_{IH}\text{ or } V_{IL}$		$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$V_{CC} = 0\text{ V}; V_I\text{ or } V_O = 3.6\text{ V}$		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current (Note 9)	$1.65\text{ V} \leq V_{CC} \leq 3.6\text{ V}; V_I = \text{GND or } V_{CC}$		40	$\mu\text{A}$
		$1.65\text{ V} \leq V_{CC} \leq 3.6\text{ V}; 3.6\text{ V} \leq V_I, V_O \leq 3.6\text{ V}$		$\pm 40$	
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$2.7\text{ V} < V_{CC} \leq 3.6\text{ V}; V_{IH} = V_{CC} - 0.6\text{ V}$		750	$\mu\text{A}$

8. These values of  $V_I$  are used to test DC electrical characteristics only.

9. Outputs disabled or 3-state only.

# 74ALVCH16240

**AC CHARACTERISTICS** (Note 10;  $t_R = t_F = 2.0$  ns;  $C_L = 30$  pF;  $R_L = 500$   $\Omega$ )

Symbol	Parameter	Waveform	Limits						Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$						
			$V_{CC} = 3.0$ V to 3.6 V		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} = 1.65$ V to 1.95 V		
			Min	Max	Min	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Input to Output	1	1.0 1.0	3.0 3.0	1.0 1.0	3.7 3.7	1.0 1.0	6.0 6.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time to High and Low Level	2	1.0 1.0	4.4 4.4	1.0 1.0	5.7 5.7	1.0 1.0	8.2 8.2	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time From High and Low Level	2	1.0 1.0	4.1 4.1	1.0 1.0	5.2 5.2	1.0 1.0	7.8 7.8	ns
$t_{OSHL}$ $t_{OSLH}$	Output-to-Output Skew (Note 11)			0.5 0.5		0.5 0.5		0.75 0.75	ns

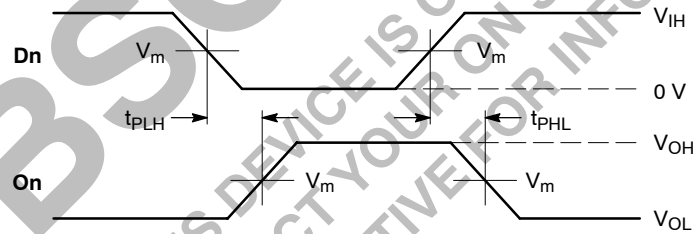
10. For  $C_L = 50$  pF, add approximately 300 ps to the AC maximum specification.

11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## CAPACITIVE CHARACTERISTICS

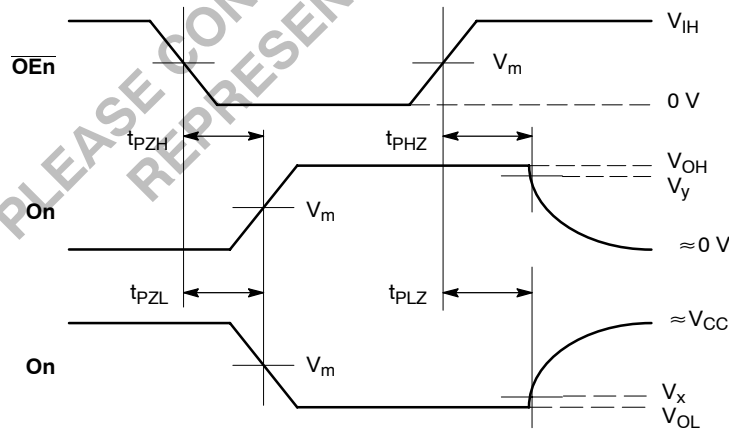
Symbol	Parameter	Condition	Typ	Unit
$C_{IN}$	Input Capacitance	(Note 12)	6	pF
$C_{OUT}$	Output Capacitance	(Note 12)	7	pF
$C_{PD}$	Power Dissipation Capacitance	10MHz (Note 12)	20	pF

12.  $V_{CC} = 1.8, 2.5$  or  $3.3$ V;  $V_I = 0$ V or  $V_{CC}$ .



**Waveform 1 - Propagation Delays**

$t_R = t_F = 2.0$  ns, 10% to 90%;  $f = 1$  MHz;  $t_W = 500$  ns



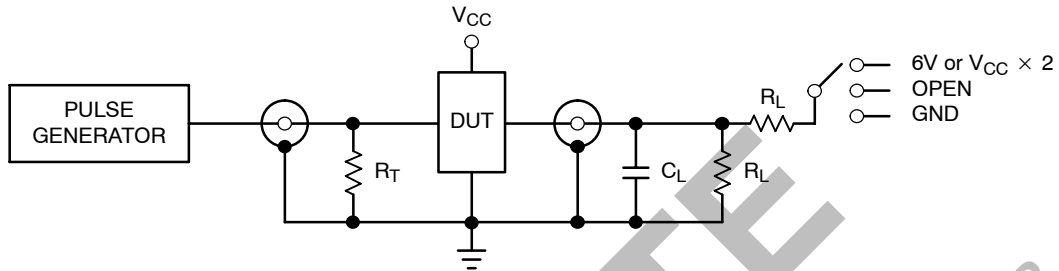
**Waveform 2 - Output Enable and Disable Times**

$t_R = t_F = 2.0$  ns, 10% to 90%;  $f = 1$  MHz;  $t_W = 500$  ns

**Figure 4. AC Waveforms**

# 74ALVCH16240

Symbol	V <sub>CC</sub>		
	3.3 V ± 0.3 V	2.5 V ± 0.2 V	1.8 V ± 0.15 V
V <sub>IH</sub>	2.7 V	V <sub>CC</sub>	V <sub>CC</sub>
V <sub>m</sub>	1.5 V	V <sub>CC</sub> /2	V <sub>CC</sub> /2
V <sub>x</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OL</sub> + 0.15 V	V <sub>OL</sub> + 0.15 V
V <sub>y</sub>	V <sub>OH</sub> - 0.3 V	V <sub>OH</sub> - 0.15 V	V <sub>OH</sub> - 0.15 V

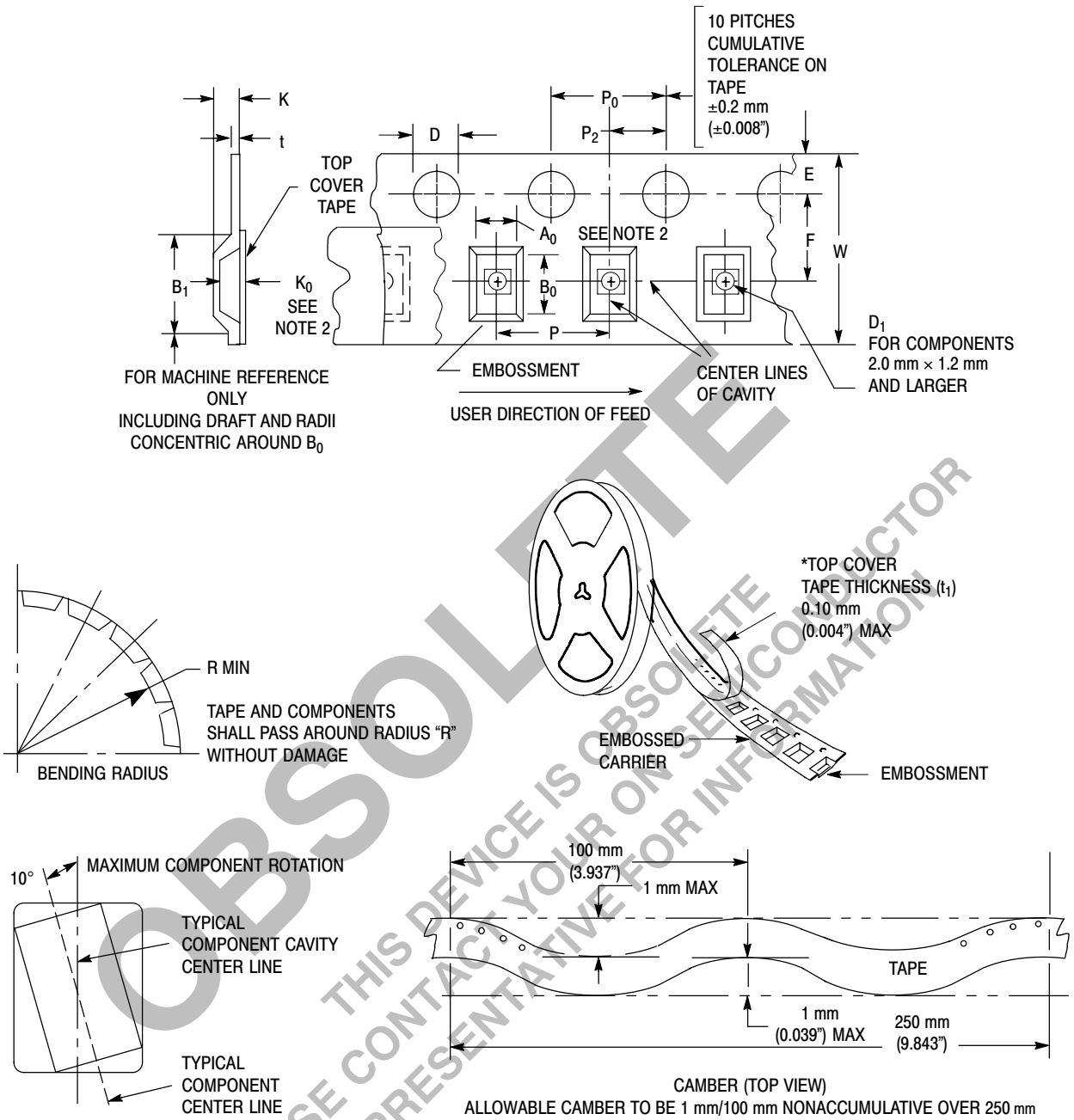


Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6 V at $V_{CC} = 3.3 \pm 0.3$ V; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2$ V; $1.8 \pm 0.15$ V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50$  pF for  $V_{CC} = 3.0 \pm 0.3$  V  
 $R_L = 500 \Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

Figure 5. Test Circuit

# 74ALVCH16240



**Figure 6. Carrier Tape Specifications**

**EMBOSSED CARRIER DIMENSIONS** (See Notes 13 and 14)

Tape Size	B <sub>1</sub> Max	D	D <sub>1</sub>	E	F	K	P	P <sub>0</sub>	P <sub>2</sub>	R	T	W
24mm	20.1mm (0.791")	1.5 + 0.1mm -0.0 (0.059 +0.004" -0.0)	1.5mm Min (0.060")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.10 mm (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 ±0.1 mm (0.63 ±0.004")	4.0 ±0.1 mm (0.157 ±0.004")	2.0 ±0.1 mm (0.079 ±0.004")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

13. Metric Dimensions Govern—English are in parentheses for reference only.

14. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

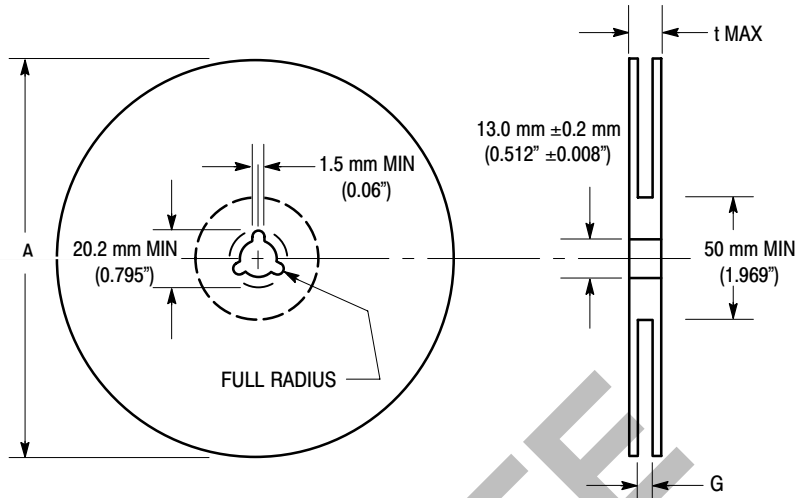


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, -0.0 (0.961" + 0.078", -0.00)	30.4 mm (1.197")

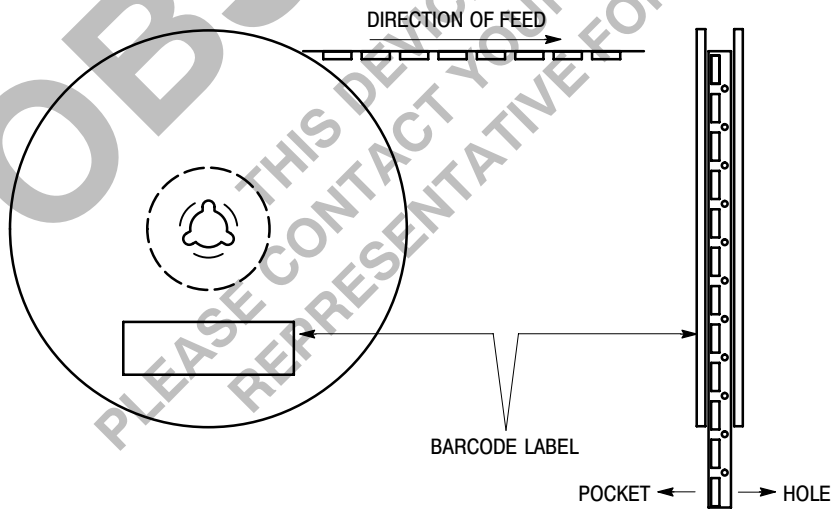


Figure 8. Reel Winding Direction



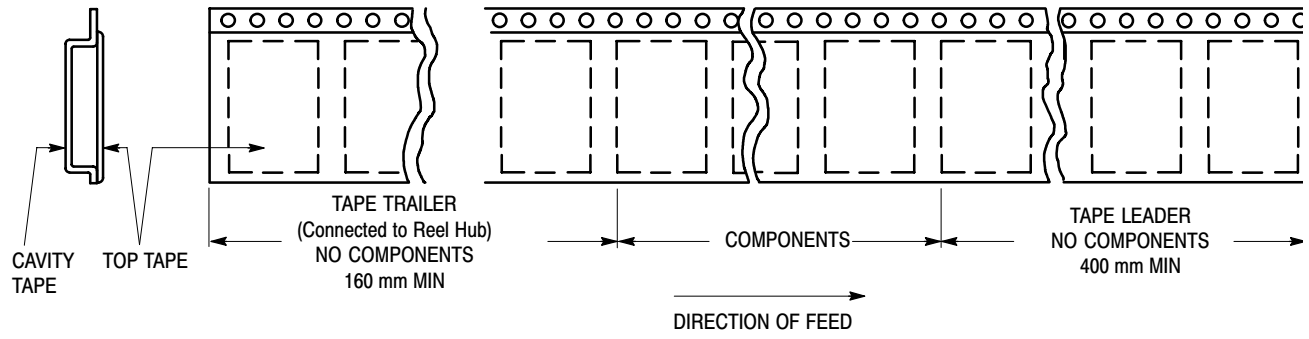


Figure 9. Tape Ends for Finished Goods

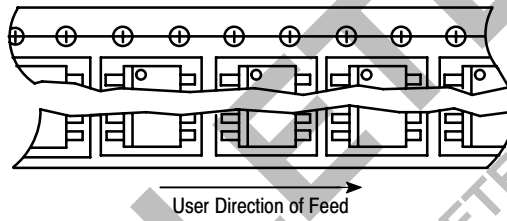


Figure 10. Reel Configuration

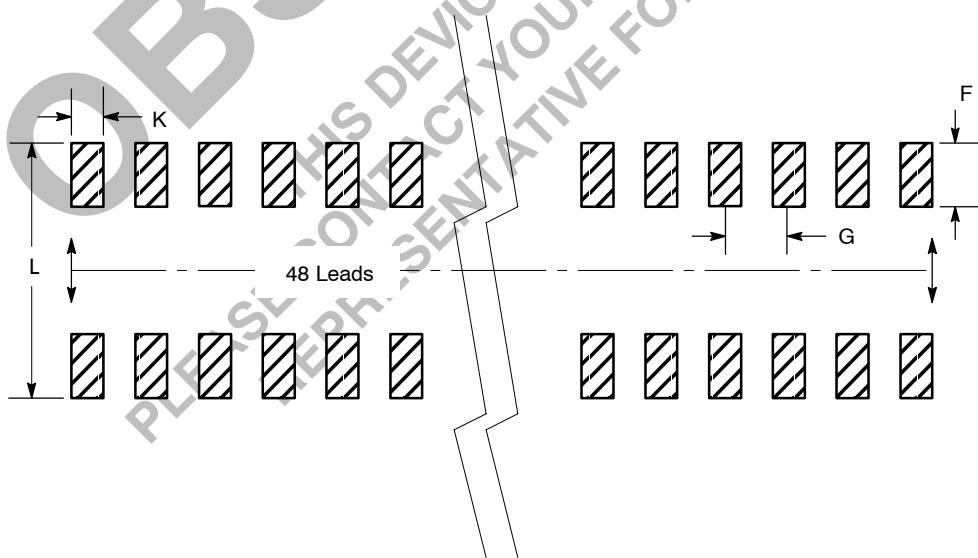
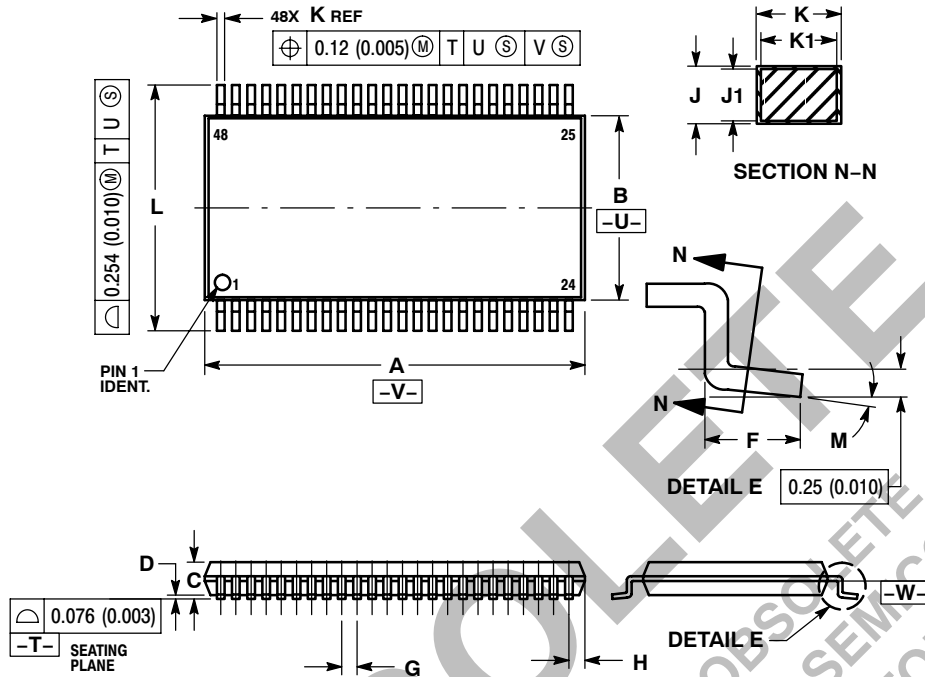


Figure 11. Package Footprint

# 74ALVCH16240

## PACKAGE DIMENSIONS

TSSOP  
DT SUFFIX  
CASE 1201-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative